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08/082,328	06/24/1993	THOMAS F. KNIGHT	7828003	4177

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EXAMINER

VIGUSHIN, JOHN B

ART UNIT PAPER NUMBER

2827

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

08/082,328

Applicant(s)

KNIGHT ET AL.

Examiner

John B. Vigushin

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,28,37-48,52-59,102,143,144,146,147 and 210-224 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 44,102,143,144,146,147 and 217-222 is/are allowed.
- 6) ☒ Claim(s) 1,28,37-42,45,53-59,210-212,223 and 224 is/are rejected.
- 7) ☒ Claim(s) 43,46-48,52 and 213-216 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. The present Office Action is responsive to Applicant's amended Response filed July 15, 2002. The Examiner acknowledges the amendments to Claims 1, 28, 44, 46, 53, 59, 102, 218, 220, and the addition of new Claims 223 and 224. Accordingly, Claims 1, 28, 37-48, 52-59, 102, 143, 144, 146, 147 and 210-224 are now pending in the instant amended Application.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

*Koepf (US 5,138,436)

*Moresco et al. (US 5,404,265)

*Already of record in the instant Application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily

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published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims **1**, **28**, 37-39, 41, 42, 53-55, 58, **59**, 210-212, **223** and 224 are rejected under 35 U.S.C. 102(e) as being anticipated by Koepf.

As to Claim **1**, Koepf discloses, in Figs. 1 and 4, a substrate 28; a GaAs—i.e., semiconductor—chip 18 (col.1: 20-24; col.8: 59-61); means for powering chip 18 (col.5: 30-34); means for capacitively signaling (pad 23 on chip 18 and the pad associated with signal line 31 on substrate 28; see Fig. 1 and col.5: 43-47) between chip 18 and substrate 28 in the coupling zone 62 (Fig. 4; col.7: 31-50); signal leads 31 and 52 connected on substrate 28 and chip 18, respectively, to the means (i.e., the above-mentioned chip and substrate pads) for capacitively signaling (Fig. 4; col.7: 31-50).

As to Claim 37, Koepf further discloses that means for capacitively signaling comprises the first and second half-capacitors, the first half-capacitor 23 being associated with chip 18 and the second half-capacitor (pad at the end of transmission line 30; see Fig. 1) associated with substrate 28; the first and second coupled half-capacitors comprising effectively overlapping conductive regions at coupling zone 62, separated there by a gap (Fig. 4).

As to Claim 38, Koepf further discloses that the conductive regions comprise pad 23 on chip 18 and the pad at the end of transmission line 31 on substrate 28, either of which conductive regions (i.e., pads) comprises a plate of the means for capacitively signaling.

As to Claim 39, the capacitance of the means for capacitively signaling *inherently can* be varied by changing the effective area of overlap between the conductive regions at coupling zone 62.

As to Claim 41, Koepf discloses that the gap 25, which includes the gap between chip 18 and substrate 28 at coupling zone 62, is at least partially filled with a dielectric, i.e., air (Fig. 4; col.7: 46-50).

As to Claim 42, Koepf discloses an air dielectric in the gap 25 which is *inherently* uniform in such a small quantity as that provided in the uniformly sized gap 25 within interconnect package 10 (col.6: 46-66) because if the air dielectric were not uniform, there would be random errors generated in the electric field strength between said means for capacitive signaling, i.e., noise due to unpredictable fluctuations in the air dielectric constant.

As to Claim 53, Koepf further discloses a plurality of coupled half-capacitors 23 (on chip 18) and corresponding pads at the ends of transmission lines 31 (on substrate 28), a substantial area of chip 18 and a substantial portion of the area of substrate 28 overlapping chip 18 being covered with substantially overlapping half-capacitors (Figs. 1 and 4; col.5: 15-25; col.5: 56-col.6: 3).

As to Claim 54, Koepf further discloses at least one half-capacitor 23 on chip 18 is connected to a chip ground, power, or other common reference signal by means of electromagnetic, i.e., contactless, coupling (col.5: 15-25; col.7: 34-42).

As to Claim 55, Koepf further discloses at least one half-capacitor (the pad at the end of transmission line 31; col.5: 57-59) is connected to a substrate ground, power, or

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other common reference signal by means of electromagnetic, i.e., contactless, coupling (col.7: 21-24 and 37-42).

As to Claim 58, Koepf further discloses that first half-capacitor 23 overlays circuitry (col.5: 15-25).

As to Claims 210 and 211, Koepf further discloses that, a transmission line 52 and a transmission line 31 are coupled to each of a first and second means for capacitively signaling, each means for capacitively signaling comprising a pad 23 on chip 18 and a pad at the end of the transmission line 31 on substrate 28 (Figs. 1 and 4; col.5: 56-59; col.7: 34-42).

As to Claim 212, Koepf discloses that transmission line 31 is further coupled to a conductive junction, i.e., an RF I/O interconnect 26 or other MMIC chips 18 (col.7: 21-26 and 31-42).

As to Claim 28, Koepf discloses, in Figs. 1 and 4: a GaAs--i.e., semiconductor--chip 18 (col.1: 20-24; col.8: 59-61); a substrate 28; a plurality of electronic devices implemented on chip 18 (the chip is a monolithic microwave integrated circuit--i.e., MMIC (col.4: 58-63)--which integrates a plurality of high-frequency electronic devices thereon, such as switches, logic devices and amplifiers); a signal lead of at least one of the plurality of electronic devices coupled by microstrip line 52 to a first half-capacitor 23 attached to chip 18 (Fig. 4; col.7: 34-37); a second half-capacitor (i.e., the pad at the end of transmission line 31; see Fig. 1) attached to substrate 28 and capacitively coupling a signal to the first half-capacitor 23 (Fig. 4; col.7: 37-42).

As to Claim **59**, Koepf discloses, in Figs. 1 and 4: a substrate 28; a GaAs—i.e., semiconductor—chip 18 (col.1: 20-24; col.8: 59-61); means for powering chip 18 (col.5: 30-34); means for capacitively signaling between chip 18 and substrate 28 comprising first and second coupled half-capacitors (i.e., the first half-capacitor is pad 23 on chip 18 and the second half-capacitor is the pad associated with signal line 31 on substrate 28, wherein the pads are capacitively coupled to each other in coupling zone 62; see Figs. 1 and 4, and col.7: 37-50); the first and second half-capacitors comprise effectively overlapping regions separated by a gap at coupling zone 62 (Fig. 4); an additional half-capacitor 23 associated with chip 18 (there are plural half-capacitors 23 on the chip; col.5: 18-20).

As to Claim **223**, Koepf discloses, in Figs. 1 and 4: a substrate 28; a GaAs—i.e., semiconductor—chip 18 (col.1: 20-24; col.8: 59-61); a first half-capacitor 23 attached to chip 18 (Figs. 1 and 4; col.7: 31-42); a plurality of electronic devices implemented on chip 18 (the chip is a monolithic microwave integrated circuit—i.e., MMIC (col.4: 58-63)—which integrates a plurality of high-frequency electronic devices thereon, such as switches, logic devices and amplifiers); a signal lead of at least one of the plurality of electronic devices coupled by microstrip line 52 to the first half-capacitor 23 (Fig. 4; col.7: 34-37); a second half-capacitor (i.e., the pad at the end of transmission line 31; see Fig. 1) attached to substrate 28 and capacitively coupling a signal to first half-capacitor 23 (Fig. 4; col.7: 37-42).

As to Claim 224, Koepf further discloses contacts 22 and 24 for supplying DC power to chip 18 from a source outside the chip (Figs. 1 and 4; col.4: 51-57; col.5: 26-34; col.7: 31-34).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moresco et al.

I. Moresco et al. discloses, in Fig. 1B: a semiconductor (integrated circuit) chip 10 (col.3: 44); a substrate 20; a plurality of electronic devices inherently implemented on the integrated circuit chip 10; a signal lead of at least one of the plurality of electronic devices inherently coupled to a first half-capacitor 30' attached to chip 10; a second half-capacitor 40' attached to substrate 20 and capacitively coupling a signal to first half-capacitor 30' (col.4: 44-48; note that this capacitive signaling embodiment—i.e., the microwave supply matching network—is taught as an alternative embodiment distinct from the bypass capacitor embodiment disclosed elsewhere in the patent of Moresco et al.).

II. Moresco et al. does not explicitly teach or show a signal lead of at least one of the plurality of electronic devices on chip 10 coupled to the first half-capacitor 30' of chip 10.

III. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a signal lead of at least one of the plurality of electronic devices of chip 10 to the first half-capacitor 30' of Moresco et al. in order for the chip 10 device(s) to receive the impedance-matched signal from the power supply required for the operation of chip 10.

7. Claims 40, 45, 56 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koepf.

A) As to Claims 40 and 45:

I. Koepf discloses all the limitations of base and intervening Claims 1 and 37 but does not teach that portions of chip 18 are passivated except the first half-capacitor 23.

II. Passivating layers (e.g., a resist, resin, an oxide layer, etc.) which are either deposited or epitaxially grown on an active surface of a semiconductor chip are old and well-known in the art to protect the chip circuitry from contamination and interconnection shorts.

III. Since Koepf teaches capacitive coupling (signaling) between the chip pad 23 (first half-capacitor) and the transmission line 31 pad (second half-capacitor) on substrate 28, it would have been obvious to one of ordinary skill in the art at the time the invention was made to passivate at least the chip portions carrying the wiring and pn

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junction electronic devices in order to protect the wiring and junction devices from, at the very least, environmental contamination and shorts, and furthermore, not to passivate the first and second coupled half-capacitors in order to expose them to the uniform air dielectric in the gap 25--that includes the space between the first and second half-capacitors--for ensuring the best possible capacitive coupling therebetween. The above-mentioned exemplary passivation layers (i.e., resists, resins, oxide layers) are inherently distinct from the air dielectric between the coupled first and second half-capacitors.

B) As to Claims 56 and 57:

I. Koepf discloses all the limitations of base and intervening Claims 1, 37 and 39, and further discloses that transmission line 31 terminates in a pad (i.e., the conductive region that functions as the second half-capacitor) which overlaps chip pad 23 (i.e., the conductive region that functions as the first half-capacitor), wherein the size and shape of the conductive region or pad of transmission line 31 may have different sizes or shapes for the purpose of providing satisfactory impedance matching with the chip conductive region or pad 23 at coupling zone 62 (Fig. 4; col.5: 43-55).

II. Koepf does not teach that one of the conductive regions (pads) is greater than the area of the other of the conductive regions (pads), or, has a shape that differs from the shape of the other of the conductive regions (pads).

III. However, since Koepf teaches that different sizes and shapes of the transmission line 31 conductive regions (pads) of substrate 28 may be employed to provide a desired satisfactory impedance matching (col.5: 53-55) at the coupling zone

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62 between the two waveguides (see Fig. 4; col.7: 34-42), then it would have been an obvious matter of engineering choice to one of ordinary skill in the art at the time the invention was made to configure a conductive region (pad) at the end of substrate transmission line 31 that is greater in area and different in shape than the chip conductive region (pad) 23 in order to provide the satisfactory impedance matching recognized and required by Koepf at coupling zone 62.

Allowable Subject Matter

8. Claim **44** and Claims **102**, 143, 144, 146, 147 and 217-222 have been allowed.

9. Claims 43, 46-48, 52 and 213-216 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims:

10. The following is a statement of reasons for the indication of allowable subject matter:

The patentable subject matter in each of Claims 43, 46-48 and 52 is self-evident.

As to Claim **44**, patentability resides in *a power connector extending through the dielectric*, in combination with the other limitations of the claim.

As to Claims 213 and 215, patentability resides in that *the second area is larger than the first area*, in combination with the other limitations of Claims 213 and 215, respectively.

As to Claims 214 and 216, patentability resides in that *the second pitch is larger than the first pitch*, in combination with the other limitations of Claims 214 and 216, respectively.

As to Claims **102**, 143, 144, 146, 147 and 217-222, patentability resides in **the combination of at least one signal lead connecting the plurality of semiconductor electronic devices to the first half-capacitor and contacts for supplying DC power to the first module from a source outside the first module**, in combination with the other limitations of base Claim **102**.

11. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Response to Arguments

12. Applicant's arguments with respect to Claims 1 and 28 have been considered but are moot in view of the new ground(s) of rejection.

13. The Examiner's indication of allowability of Claims 56, 57 and 59 in the previous Office Action (mailed January 15, 2002) has been withdrawn in view of the prior art relied upon in the present Office Action.

14. Moresco et al. (US 5,404,265) has been relied upon by the previous Examiner, and traversed by the Applicant, on the basis of the bypass capacitor embodiment therein. The present Examiner has relied upon the capacitive signaling embodiment in col.4: 44-48 to reject Applicant's Claim **28** in section 6, above.

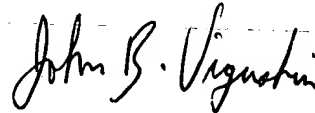
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Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



John B. Vigushin
Examiner
Art Unit 2827

jbv
October 20, 2002